# **RISC V Processor**

# by Sree Sankar E (M24EEV512)

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# **System Architecture**

The processor designed with RISC V 32I core.

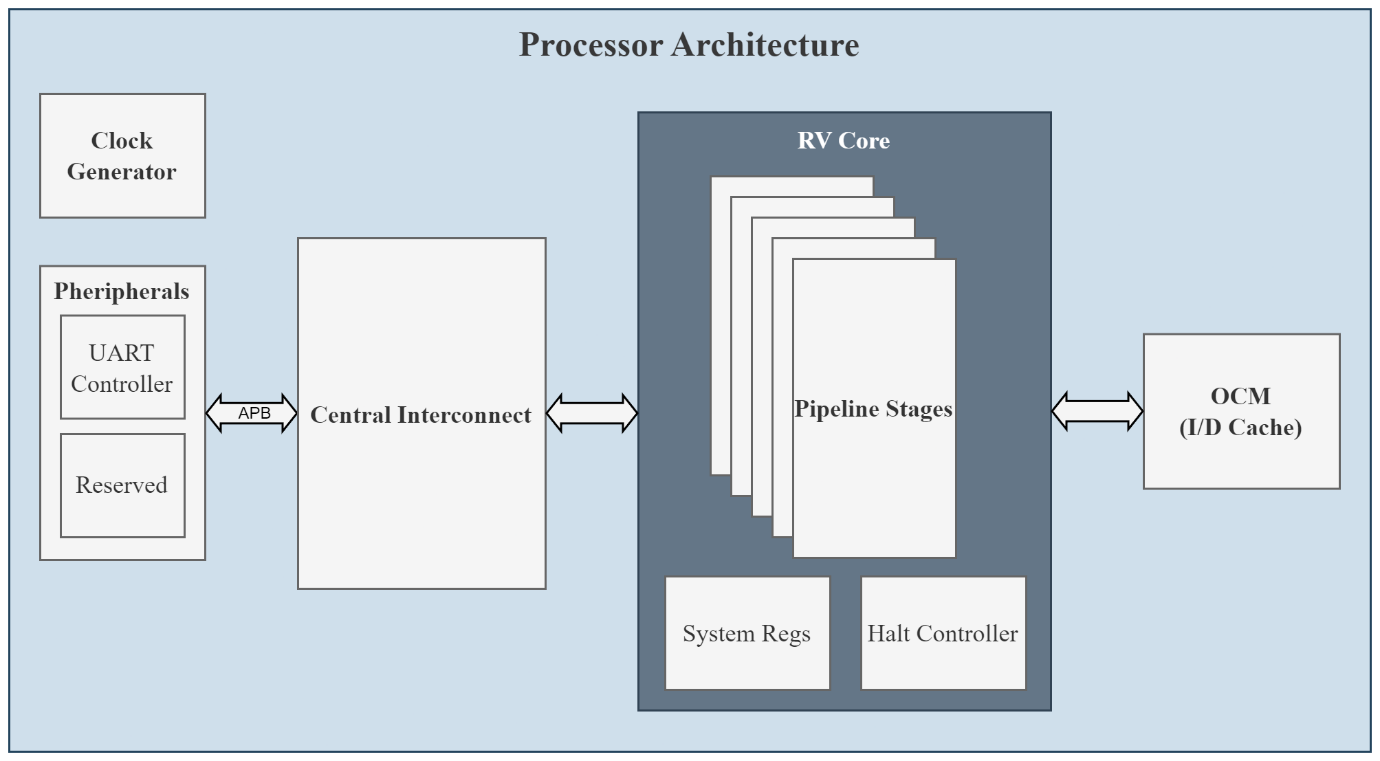


Figure 1‑1: System Architecture

# **RISC V Core**

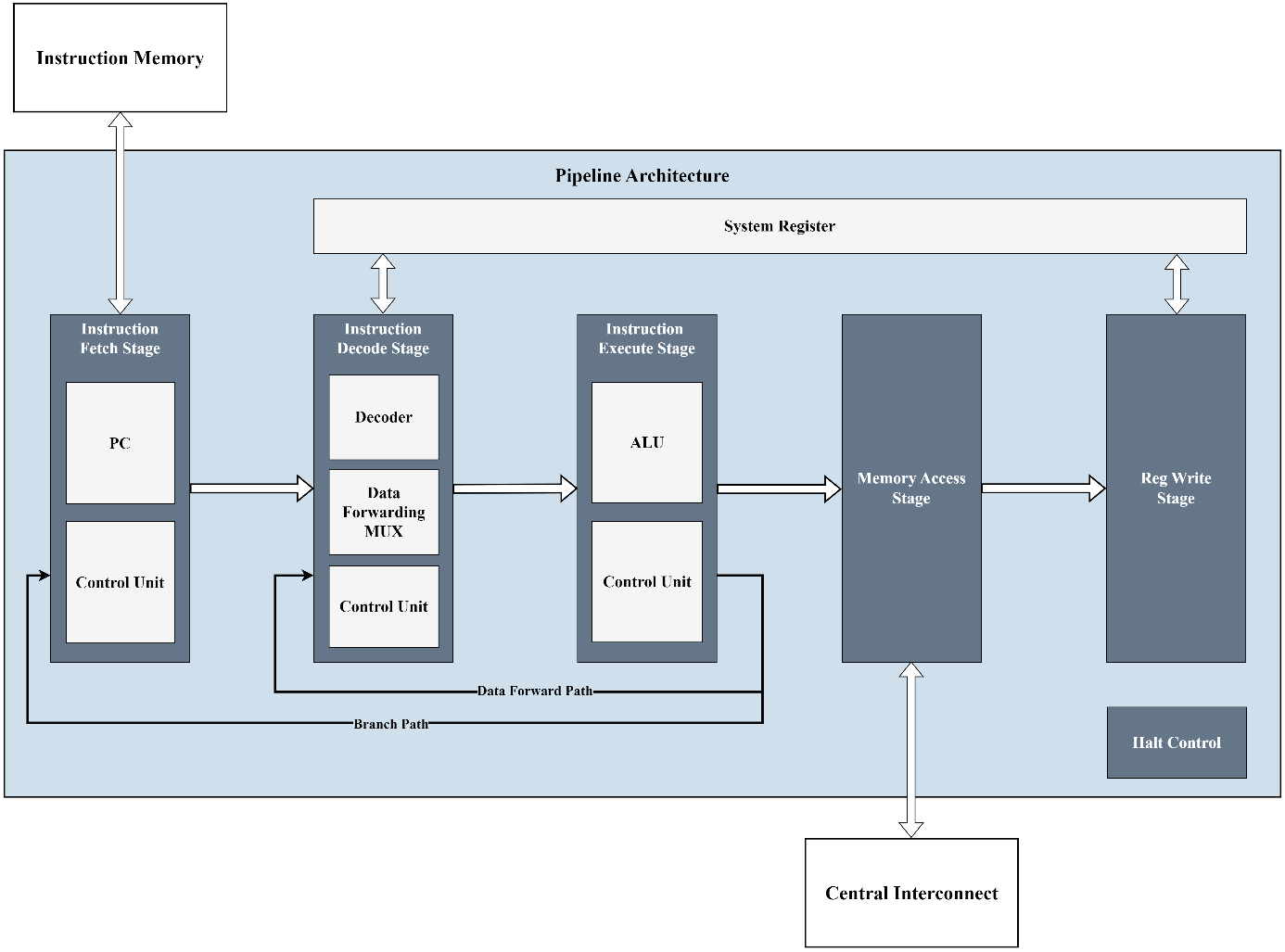


Figure 2‑1: Pipeline Architecture

Core Specification

* Architecture : RISC V 32-bit Integer
* Extension : I
* Pipeline Stages : 5
* ISA : As per RISCV ISA Manual Volume 1 20240411

*Note: Zicsr Extension, SYSTEM and MISC-MEM instruction not implemented*

# **Memory Map**

This section describes about the memory map of the processor.

|  |  |  |
| --- | --- | --- |
| **Base Address** | **Offset** | **Description** |
| 0x0000\_0000 | 0x0000\_FFFF | OCM |
| Reserved | Reserved | Reserved |
| Peripherals | | |
| 0xA000\_0000 | 0x0000\_0FFF | UART |
| Reserved | Reserved | Reserved |

Table 3‑1: Memory Map

# **Clock Generator**

It generates clock and reset for all subblock of the system. The reset for the core is synchronous active low reset.

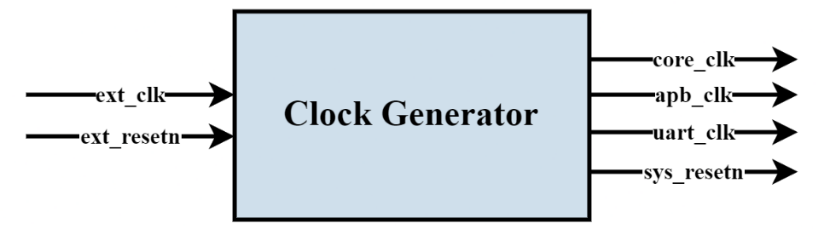


Figure 4‑1: Clock Generator Block Diagram

|  |  |  |
| --- | --- | --- |
| **Clock Name** | **Frequency** | **Description** |
| core\_clk | 100 MHz | RISC V Core Clock |
| apb\_clk | 100 MHz | APB Interconnect Clock |
| uart\_clk | 115.2 KHz | UART Clock |

Table 4‑1: Clock Frequency

# **Central Interconnect**

It interfaces the core with memory and peripheral controllers.

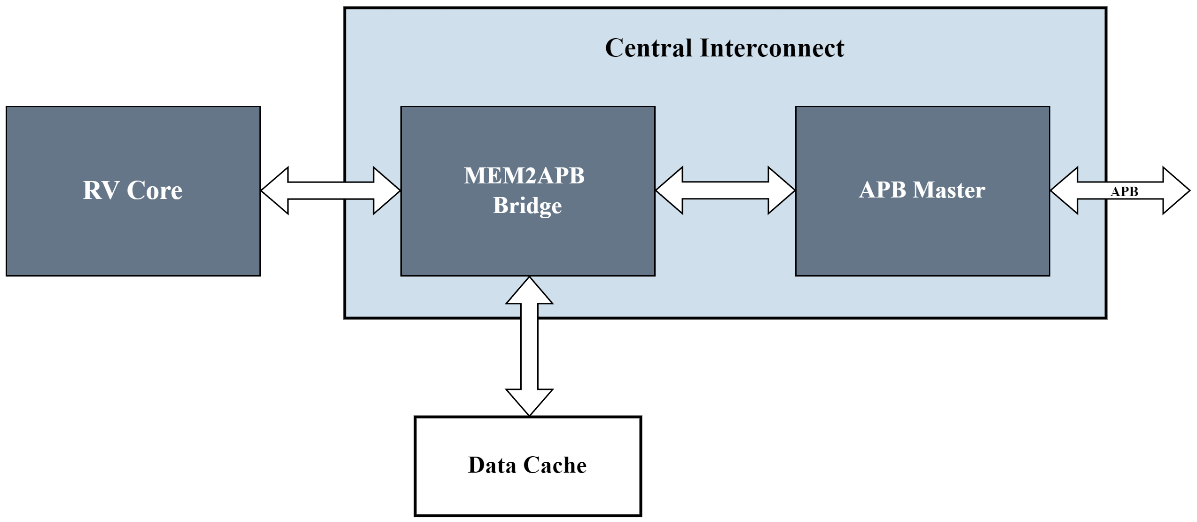


Figure 5‑1: Central Interconnect Block Diagram

**MEM2APB:** It has 2 functionalities

* Acts as memory selection mux based on memory map
* Bridge RV core memory interface to APB interface

*Note: Data handling between Core data rate and APB needs to be handled. Added NOP instruction to compensated for write APB latency.*

# **UART Controller**

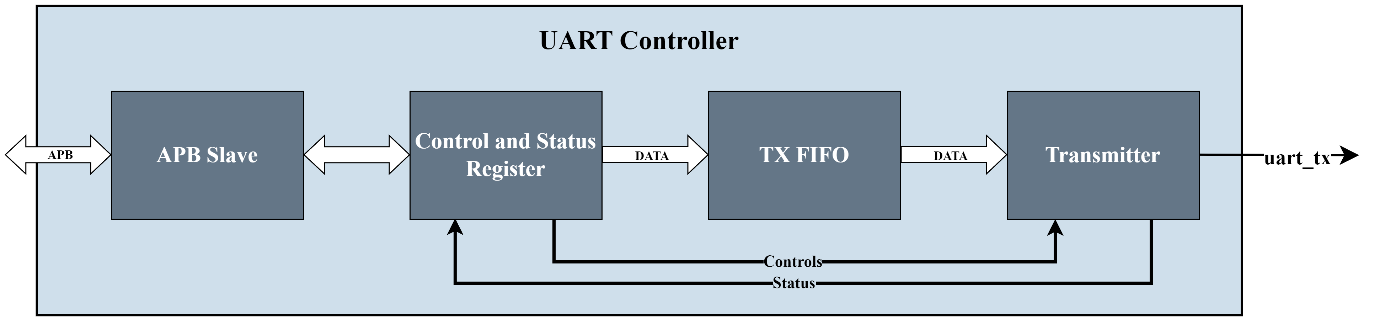


Figure 6‑1: UART Controller Block Diagram

Specification:

* Baud Rate : 115200 bps (fixed)
* Start bits : 1 bit
* Data bits : 8 bits
* Parity bit : NA
* Stop bits : 1 bit

*Note: UART RX not implemented*

This following are the registers in the UART controller

|  |  |  |
| --- | --- | --- |
| **Register** | **Offset** | **Description** |
| UART\_CTRL\_REG | 0x0000\_0000 | Control Register |
| UART\_STATUS\_REG | 0x0000\_0004 | Status Register |
| UART\_TX\_DATA\_REG | 0x0000\_0008 | Transmit Data Register |

Table 6‑1: UART Control and Status Register

**UART\_CTRL\_REG**

* Address Offset : 0x0000\_0000
* Default Value : 0x0000\_0000

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit Field** | **Bits** | **Read/Write** | **Description** |
| Reserved | 31:1 | R/W | Reserved |
| TX Enable | 0 | R/W | Transmit Enable |

Table 6‑2: UART\_CTRL\_REG

**UART\_STATUS\_REG**

* Address Offset : 0x0000\_0004
* Default Value : 0x0000\_0000

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit Field** | **Bits** | **Read/Write** | **Description** |
| Reserved | 31:1 | R | Reserved |
| TX Status | 0 | R | Transmitter Status  0: Idle state  1: Busy |

Table 6‑3: UART\_STATUS\_REG

**UART\_TX\_DATA\_REG**

* Address Offset : 0x0000\_0008
* Default Value : 0x0000\_0000

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit Field** | **Bits** | **Read/Write** | **Description** |
| Reserved | 31:8 | R/W | Reserved |
| TX Data | 7:0 | R/W | Transmit Data |

Table 6‑4: UART\_TX\_DATA\_REG

# **Design Repo**

* GIT: <https://github.com/sree-sankar/riscv_processor>
* RISC V: <https://github.com/sree-sankar/riscv_processor/tree/master/src/risc-v>

# **Validation**

Testbench based verification, SVA based verification and implementation validated on Diligent Arty A7-35T reference board with Xilinx XC7A35TICSG324-1L FPGA.

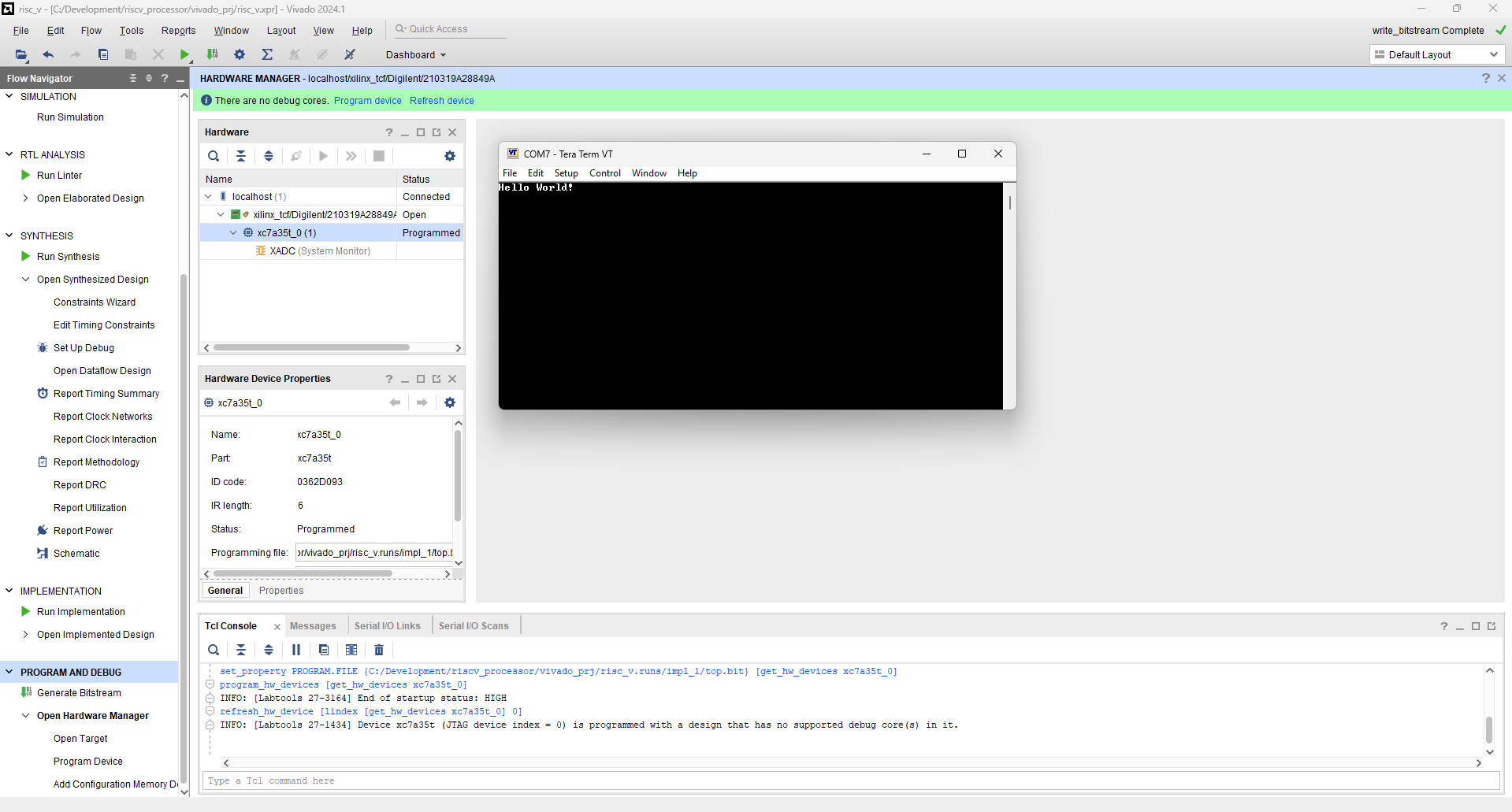


Figure 8‑1: FPGA Validation

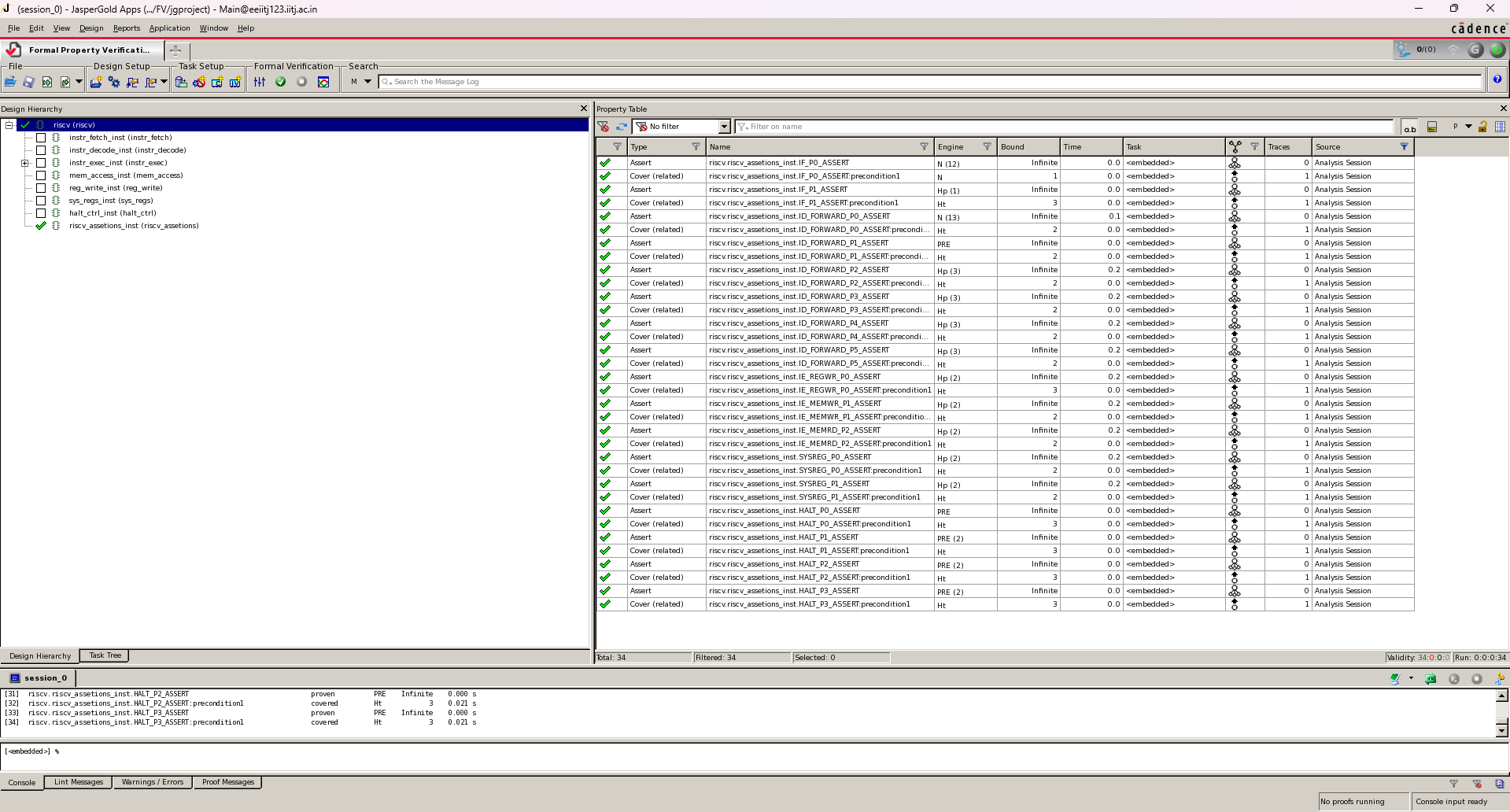


Figure 8‑2: Formal Verification Report